Int.J.HIT.TRANSC:ECCN.Vol.6: Issue 2A (2020) Page 10-20 ISSN: 0973-6875

Available Online at www.hithaldia.in/locate/ECCN
All Rights Reserved

ORIGINAL CONTRIBUTION

Digital Backend Optimization Techniques for Post Route and Sign-off Challenges in ASIC Design

Nikhil Danthamala[1], Vijitaa Das[2], Vishwnatha Hanchinal[3]

[1] *Department of Electronics and Communications Engineering, National Institute of Technology, Goa, India*

[2] *Department of Electronics Design Technology, National Institute of Electronics & Information Technology, Calicut, India*

[3] *Design Engineer, NXP Semiconductors, USA*

ABSTRACT

With the advancement of technologies, complexity in IC design has led to different Routing problems. And hence by using multiple patterning methodologies and techniques, it could not help much in reducing timing closure issues and electro migration problem at Sign-off Stage. The real goal of ASIC is to tape-out at theright time without any design constraints. Optimization of timing and minimizing IR drop in VLSI is essential to meet these challenges. This paper proposes improved implementation techniques to overcome Timing and IR-drop challenges which can be applied on each stage of Place and Route flow in ASIC design. The proposed methodologies can be implemented in any existing physical design flow to achieve the target.

KEYWORDS: Timing optimization, Critical Nodes, IR drop analysis, PG Pattern, ECO Optimization

1. INTRODUCTION

As the Technology scaling is happening rapidly, there are areas in the Physical design where we need to concentrate more to avoid chip breakdown. With the trend of smaller process nodes, to achieve design closure becomes quite challenging.[2] Detection, analysis and removing the issues is a critical job, especially in early stage of the design. In recent studies, it has been reported that while focusing on low power IC design, performance of chip is getting badly affected. Couple of such issues arises when important areas are overlooked that include Targeting Critical nodes, which causes timing critical violations and voltages (IR) drops occurrences in the design. [4]As each stage in the physical design has its own set of challenges and every stage depends on previous stage's yield generated at physical verification closure. The existing techniques are not beneficial enough to meet these checks.

In this paper, section I will discuss about timing closure constraints and section II will discuss about how conventional methods are failing to reduce IR drop hotspots. In section I, an improved timing optimization technique is proposed whose purpose is to focus more on critical nodes after Post Route stage and optimize them by providing worst negative slack (WNS), area, power, maximum transition violation improvements with minimum disturbance to design's routing.

In section II, an improved IRdrop optimized technique is proposed to reduce the IR drop hotspots and Dynamic IR drop related challenges. Its purpose is to add more stripes to reduce the resistances of the existing power grid which are causing higher IRdrops. Proper analysis and optimization of functional blocks is done after each stage of Physical design flow, has shown in this paper. This work concentrates on overcoming all the challenges

*Corresponding Address: nikhildanthamala@gmail.com

during tape out of the design to meet the final Sign-off checks.

2. LITERATURESURVEY

Physical design is involved in improving several parameters such as timing, power, area, signal integrity, reliability, etc. And while improving these parameters, they show some negative impact on timing. Timing violation is hard to identify during initial stages of the design, which later during tape-out creates real violations. This can eventually cause poor performance during functionality of IC. [6]

According to Moore's Law, the number of transistors is increasing exponentially with release of every latest IC design, computational complexity of timing closure is also increasing.

Before starting the optimization experiment, the basic unit is to understand the overall structure of the functional unit block. In the design, we need to identify the power-hungry area and the timing critical path. Sometimes the timing critical path can also lead to increased power. Once the circuit is analyzed, we need to understand how to optimize power and timing, and how to use various methods to converge timing and power gain. To get high quality performance from the design, it is necessary to make sure that various optimization techniques used to achieve timing convergence and gain power, should not have any negative impact on the overall efficiency of the design.[7]

With the increase in clock frequency, duration of signal transmission decreases and hence it fails to meet timing constraints of the design. In advanced technology nodes for achieving low power consumption, some important techniques like clock Gating, multi-threshold voltage, power domains etc. are also used. Hence as a result it creates conflict between the trade-offs of the timing constraints. [10]

Due to Dynamic IR drop, robustness caused by the power when it is distributed to the chip and can also effect timing closures by using switching patterns.[11] Rising IR drop on clock and/or on the data paths leads to timing violations. During at-speed scan testing, excessive switching activity causes huge current flow on power/ground network and increasing IR drop ,as a result gives rise to timing failure of the chip. [12]

3. METHODOLOGY

A. Optimization of Targeted Critical nodes in the design

The purpose of this optimization technique is to concentrate only on the critical nodes specified in a text file provided by the user, which will be fed to the tool for its reference to apply optimization to only those nodes that have been provided. User should create a text file specifying only those selected nodes which are creating timing critical violations in the design.

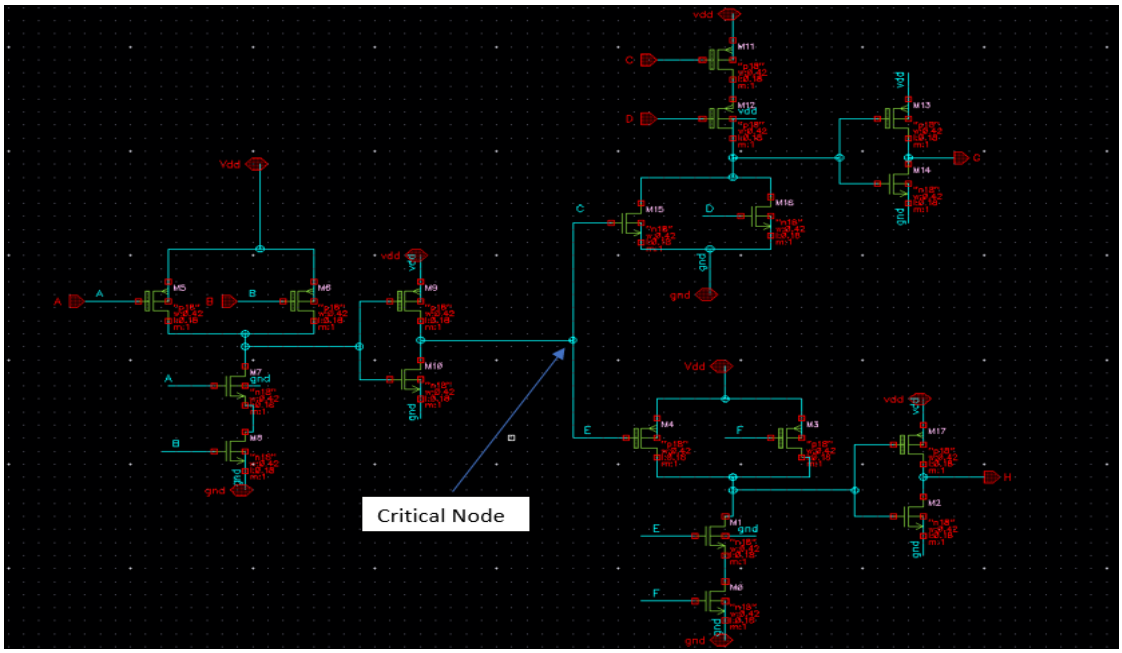

Figure 1: Critical nodes

Critical node is basically a node through which output of a gate is shared with two other gates simultaneously, making those paths setup and hold critical.

Node selection is done by referencing instances, nets, and paths involving critical nodes to pass to the software through text file to be optimized directly. The below flows will help figure out how the selection of critical nodes is done and how the critical nodes can be optimized.

In the above flow, the block inside the red dotted line refers to the things done by EDA tool internally, so provided blocks outside the dotted lines hould bed one by the user and invoke it to the tool again. Selecting critical nodes is based on two operations one is Checking Placement and second one is checking DRC. These two operations will give us a good idea about nodes which are violated and needs immediate fixing.

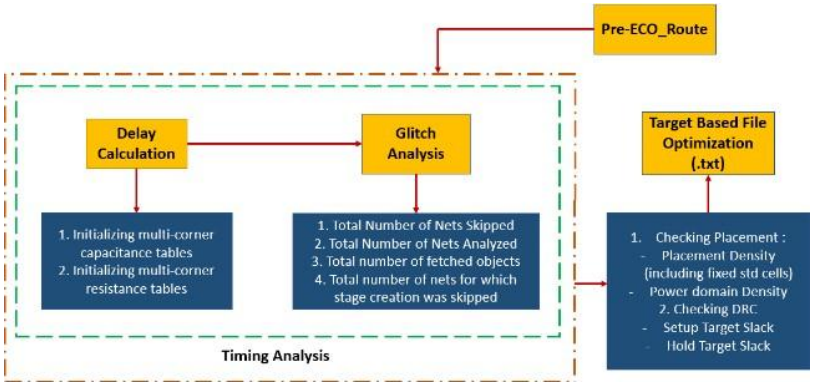

Figure 2: Critical node selection

Target based text file will contain the following information which is concluded from the two operations done.

```
NETS : {net1} {net2} {netN}
FROMTOS : {fromTerm1 toTerm1} {fromTerm2 toTerm2} {fromTermN toTermN}
INSTS : {inst1} {inst2} {instN}
PATHS : {endpoint1} {endpoint2} {endpointN}
```

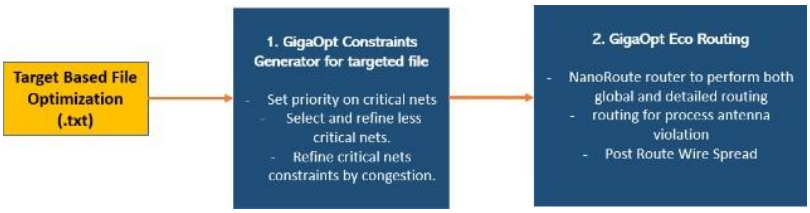

Figure 3: Optimizing targeted critical nodes

Targeted text file is now fed to the Giga Opt Constraints Generator which sets priority to the nodes in the file followed by refining the nodes with respect to the congestion as well. Later sent to the GigaOpt Eco routing which uses Nano Route to perform global and detailed routing which adjusts the setup and hold timings of the nets causing nodes to clear out of criticality.

B. Detection and optimization of IR drop

On deep sub-micron CMOS technologies, the problem after voltage (IR) drop on the power rails becomes significant. Static IR drop occurs when constant current flows through poor network with varying resistance. In other words, Static IR drop occurs when circuit is not in steady state. Unlike static IR drop, Dynamic IR drop depends on switching rates of instances.

Conventional IR drop analysis used to generate higher Dynamic IR drop at the sign-off stage and hence failed to meet the demand of accuracy and reliability from advanced process nodes. To increase speed in design, timing closure and IR drop hotspot mitigation is essential. The main motto is to minimize IR drop by identifying the hotspots where huge drop of voltage occurs which is more than threshold of an IC at early stage to prevent from achieving the targeted performance.

Traditionally, when IR-drop gets detected during tape out, the flow would be returned back to the implementation stages where iterations were done again to fix the issues. By introducing, detection of IR-drop ECO flow, sign-off clean can be achieved.

By applying Cell Spreading and cell padding technique on the design, most of the violations are addressed and can be fixed, but still some violations are left out which further creates IR drop hotspots.

First, user needs to identify the hotspots. Then, PG patterns are applied on that blocks. These patterns are specified and controlled by the user.

The construction of pattern would be done as shown below:

-pattern_file <*filename*>
-pattern_map { {*irdrop_value1 pattern_name1*} {*irdrop_value2 pattern_name2*}...}
[-write_pattern_template <*filename*>]
[-area <x1 y1 x2 y2>]
[-tile_row_column {x y}]
[-tile_size {x y}]
[-number_region *value*]
[-boxes_file <*filename*>]

PG patterns should consist of several elementary groups such as different metal layer ranging from M0 to M15, nets, etc. specified by pattern name and file. For our design, we used M0 to M5 for power planning.

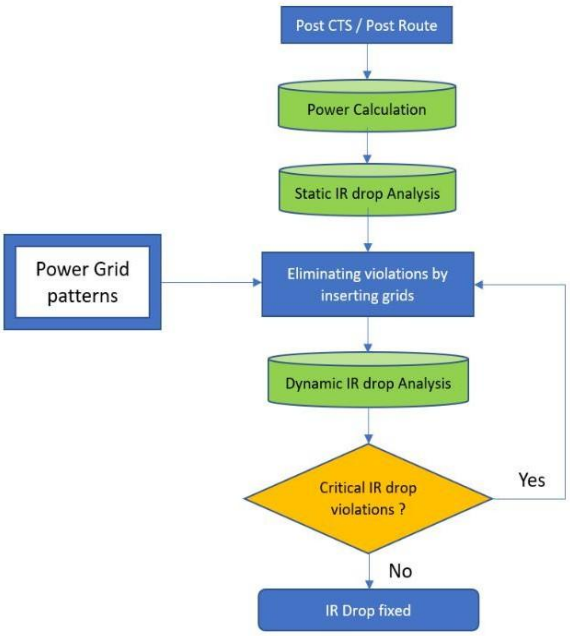

Figure 4: Insertion of Power Grid stripes flow

In the above flow, as it is shown, when the design is fully placed, after post CTS and post Route stage the power calculations will be done. Using leakage power, the static IR analysis is done. While doing Static IR drop analysis, it will detect the violations and will try to eliminate and fix them by inserting power grids from the patterns that are defined by users according to the design. During dynamic IR drop analysis, user needs to check whether there are critical violations. If yes, then they need to first identify all those grids which are causing more IR drop. At this stage, violation soccer mostly due to increase via layers stacking to fix some of these violations. By generating Resistance of Least Resistive Path (RLRP) report,

suitable metal layer can be chosen to achieve least IR drop. This will help to distribute the power on the network efficiently. Once violations are fixed, user can proceed for ECO routing.

After post route stage, to meet the IR drop margin by eliminating all the real violations remains a complex task. Some remaining violations will finally affect timing paths during sign-off checks. This is the time when user should trace out the sensitive paths which can be the real reasons for remaining violations. STA will help to identify those critical paths that are caused by the cells/instances which are sensitive to power, voltage, resistance, timing and user-defined paths. This analysis will be performed by conventional VDD Margin on cells. In this flow, the software is aware of the delays along the path and the delays of the path which are in the neighborhood. It creates switching scenarios that are sensitive to timing slack and critical timing path. It identifies proximity aggressors around voltage and critical sensitive instances based on PG resistance and timing analysis.

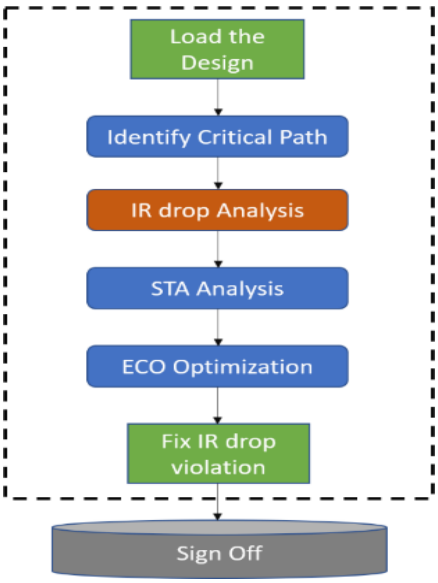

Figure 5: Optimization of IR-sensitive ECO flow

So, this analysis will be done as follows:

i. User needs to load the input designdatabase.

ii. Then needs to detect the timing violated criticalpaths.

iii. During IR drop analysis, it is necessary to report the IR drop hotspots and the worst violated victims and aggressornets.

iv. Then here, ECO optimization will be done. To fix setup and hold violations, resizing of cells and their aggressors, buffer insertion or deletion, swapping of cells are performed in ECO fixingstage.

v. Finally, it will recheck for criticalpaths.

vi. Then software will create a database to store the fix IR- awaretiming.

4. RESULTS

C. Optimization of Targeted Critical nodes in the design

Table I lists important parameters of timing analysis like WNS, TNS for setup and hold modes, which clearly states that the design has lots of timing critical nets and paths, which needed to be optimized for the design to pass timing closure.

Table I: Timing Optimization in the design before using Targeted Optimization

Before applying Targeted opt	SETUP MODE				HOLD MODE			
	All	Reg2Reg	Reg2Cgate	default	All	Reg2Reg	Reg2Cgate	default
WNS (ns)	-35.503	0.897	30.550	-35.896	-77.432	-8.987	-60.505	-146.862
TNS (ns)	-58.000	0.765	0.000	-58.000	-116.839	-7.743	-55.765	-180.763
All paths	9085	8541	36	508	9085	8541	36	508

So, after applying Targeted optimization Table II shows results much more sophisticated compared to Table I where timing is satisfied to an extinct where design can pass timing closure.

Table II. Timing Optimization in the design after using Targeted Optimization

After applying Targeted opt	SETUP MODE				HOLD MODE			
	All	Reg2Reg	Reg2Cgate	default	All	Reg2Reg	Reg2Cgate	default
WNS (ns)	-0.675	0.000	0.000	-0.675	-13.513	-0.572	-26.257	-59.297
TNS (ns)	-21.855	0.000	0.000	-21.855	-46.400	-0.777	-56.550	-102.023
All paths	8846	8349	22	475	8846	8349	22	475

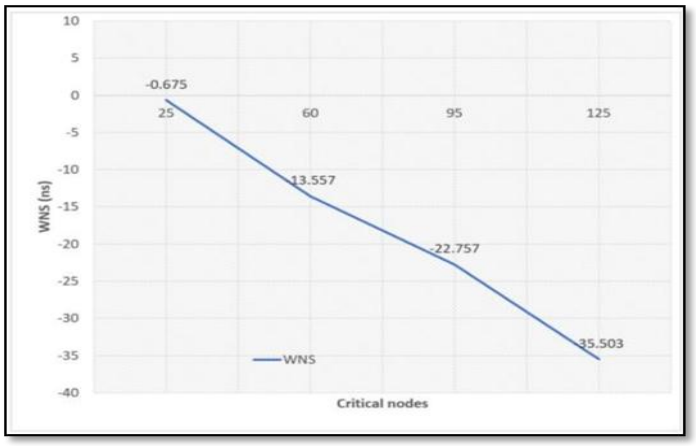

Figure 6: Comparison of Timing Optimization

The graph (Figure 6.) shown below illustrates the curve of optimization before and after targeted Optimization. Less WNS with lesser critical nodes is an optimized design after applying Targeted Optimization. The critical nodes on Y-Axis are obtained from the design by referencing to the instances, paths and critical nets.

D. Detection and optimization of IR drop

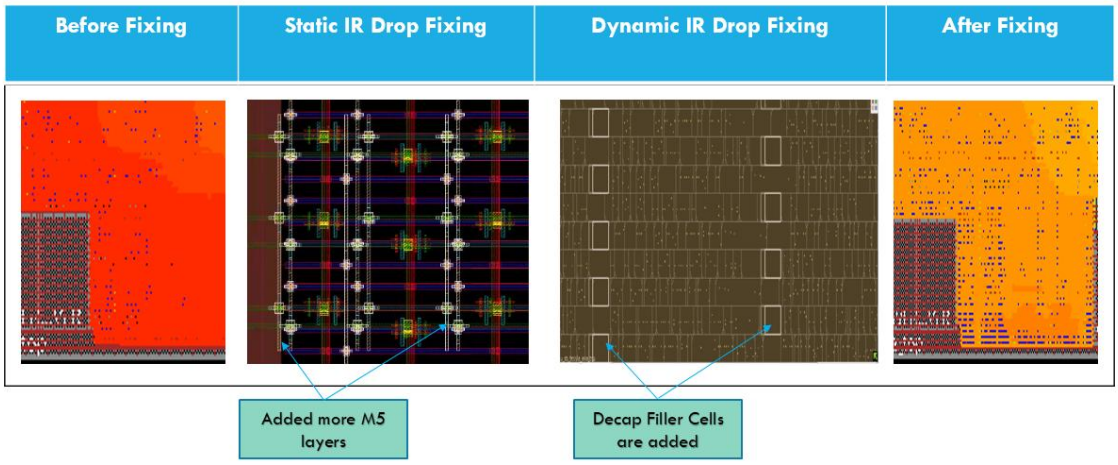

Figure 7: IR drop hotspots in the design

Clearly Figure 7 shows that huge IR Drop represents red colored hotspots over standard cell area. As IR drop is more i.e., voltage supplied to the standard cells is not 100 % due to drop, which makes the standard cells to establish output slowly due to reduced voltage supply. As output establishment is delayed, this affects the timing of those IR drop paths as well. Causing timing violations in the design establishing WNS and path violations leading to chip failure. To fix Static IR drop, we add more parallel Metal 5 (M5) layers. The purpose of adding more metal 5 layers is to reduce the resistivity of cell instance that restricts the flow of current towards the voltage supply. To fix dynamic IR drop, we added DECAP (Decoupling Capacitors) Cells. These are added in parallel to the standard cells for reducing IR drop. The capacitor acts as power storage units. These are temporary capacitors which are added in the design between power and ground rails to counter the functional failure due to Dynamic IR drop.

Table III: IR drop Analysis based on Critical Instances

	No. of Critical Instances		
IR drop(V)	**Before using PG Pattern**	**After using PG Pattern**	**After ECO optimization**
0.030-->0.040	555	310	165
0.040-->0.050	415	232	58
0.050-->0.060	318	155	17
0.060-->0.070	303	67	2
0.070-->0.080	257	29	0
0.080-->0.090	255	18	0
0.090-->0.100	182	3	0
0.100-->0.110	157	0	0
0.110-->0.120	148	0	0
0.120-->0.130	75	0	0
0.130-->0.140	21	0	0

Table IV: IR drop Improvement after applying PG pattern and ECO Optimization

	Baseline	**After using PG pattern**	**After ECO optimization**
IR drop >30 mV	2686	814	242
WNS (ns) for all	-0.675	-0.612	-0.612
TNS (ns) for all	-21.855	-21.828	-21.828

From the above two tables, it is analyzed that violated instances have been reduced from 2686 to 814 after applying PG metal stripes, and further violations decreased to 242 after STA ECO optimization. It has been observed that addition of metal layers on power grids are improving WNS and a negligible change to TNsS whereas after ECO optimization, timing is not getting impacted.

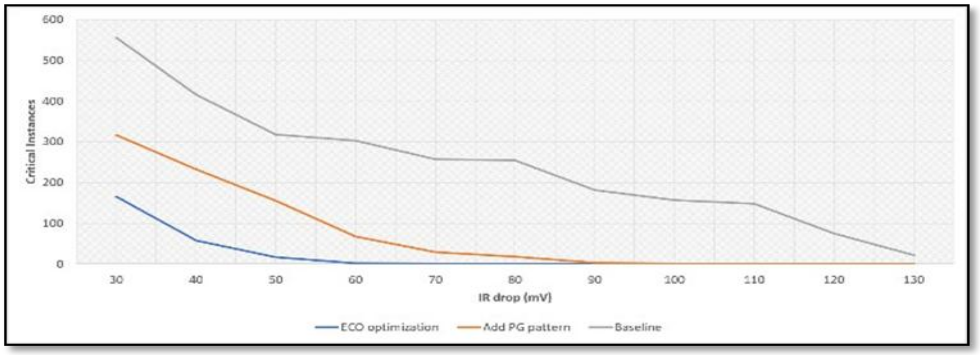

Figure 8: Comparison of IR drop optimization

Above graph demonstrates with the decrease of critical instances by utilizing user-defined pattern and ECO optimization, violations are fixed at high rate.

E. Runtime Comparison

Table V shows the runtime of the design with and without Targeted Optimization. The experiments are run on Cadence In novus Stylus. Targeted Optimization with text file took 50 secs to parse the data. The Post route Optimization step without Targeted OPT is direct optimization of design by considering all the nodes to be critical and trying to optimize the setup and hold timing, so it scans all the nodes in the design to find critical nodes which takes moretimei.e.,9mins.But with Targeted OPT we'll be providing the critical nodes through text file, so the tool need not to search again for nodes as we are already providing,hencetimeislessi.e.4mins.Theen tirerun time of designs is also mentioned in the table.

Table V: Runtime Comparison

Circuit Design	Without Targeted OPT	With Targeted OPT
Parsing Data	1.22 mins	50 secs
Post Route Optimization	9 mins	4 mins
Design Runtime	1.05 hrs	52mins

5. CONCLUSION

In this paper, sign-off issues due to critical nodes, IR drop were addressed and provided with a possible and efficient solution. Approaches through a set of techniques for analyzing and fixing the violations as adopted in our design is beneficial for robustness of power grid. Also, we have discussed how violated timing paths can cause more IR drop, which later fails to meets ign-off checks. The flow is also beneficial for reducing runtime, and simultaneously increasing accuracy and speed.

REFERENCES

[1] Lienig, Jens & Thiele, Matthias. (2018). The Pressing Need for Electromigration-Aware Physical Design. 144-151.10.1145/3177540.3177560.

[2] U. Gandhi, I. Bustany, W. Swartz and L. Behjat, "A Reinforcement Learning-Based Framework for Solving Physical Design Routing Problem in the Absence of Large Test Sets," 2019 ACM/IEEE 1st Workshop on Machine Learning for CAD (MLCAD), Canmore, AB, Canada, 2019, pp. 1-6, doi: 10.1109/MLCAD48534.2019.9142109.

[3] Jayateertha Karekar, Ramana Reddy, "Physical Design Implementation of a complex IP core aimed at area optimization ", 2016 IRJET Bangalore, India, 2016,e-ISSN:2395-0056Volume:03Issue:07|July- 2016, p-ISSN:2395-0072

[4] J. Washak, C. Alexandru and D. Zhu, "DevelopmentofanAutomaticBidirectionalWireless Charging System for Mobile Devices," 2019IEEEWireless Power Transfer Conference

(WPTC), London, United Kingdom, 2019, pp.380-384,doi:10.1109/WPTC45513.2019 .9055552.

[5] Nishi. G. Nampoothiri, "EFFECTS OF CROSSTALK ON INTERCONNECTS" in journal of Science, Technology & Management, Volume-08 No.02 April-June 2015, ISSNNO:0974-8334.

[6] L. A. Hey, "Power Aware Smart Routing in Wireless Sensor Networks," 2008 Next Generation Internet Networks, Krakow, 2008, pp. 195-202, doi: 10.1109/NGI.2008.33.

[7] J. U. Kidav, D. N. M. Sivamangai, D. M. P. Pillai and S. G. Sreejeesh, "Design and Physical Implementation of Array Signal Processor ASIC for Sector Imaging Systems," 2019 32nd International Conference on VLSI Design and 2019 18th International Conference on Embedded Systems (VLSID), Delhi, NCR, India, 2019, pp. 448-453, doi: 10.1109/VLSID.2019.00095.

[8] C. Condrat, P. Kalla and S. Blair, "A methodology for physical design automation forintegrated optics," 2012 IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS), Boise, ID, 2012, pp. 598-601, doi: 10.1109/MWSCAS.2012.6292091.

[10] W. J. Dally, C. Malachowsky, and S. W. Keckler, "21st century digital design tools," in Proceedings of the 50th Annual Design Automation Conference, ser. DAC'13.NewYork,NY:ACM,2013,pp.94:1–94:6.

[11] Vishweshwara, R. Venkatraman, R.Udayakumar, H. Arvind, N.V., "An Approach to Measure the Performance Impact of Dynamic VoltageFluctuations Using Static Timing Analysis", VLSI Design, 2009 22nd International Conference on Publication Date:5- 9 Jan.2009.

[12] L.-T. Wang, C.-W. Wu, and X. Wen, Editors, VLSI Test Principles and Architectures: Design for Testability, San Francisco: Morgan Kaufmann,2006.