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ORIGINAL CONTRIBUTION

Design of Hybrid Full Adder by Exploring New XOR and XNOR Gates

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ABSTRACT

In this paper, novel circuit for FULL ADDER are proposed by new XOR or XNOR gates. The conventional design of XOR or XNOR gates shows that the not gate in the schematic has drawback. So the schematic designs are proposed by using new XOR or XNOR gates .The designed schematics are specified in factors of speed, power and PDP. We proposed six new hybrid full adder schematics by new XOR or XNOR gates. Each designed schematics has its own specification in terms of energy consumption, delay, PDP. To simulate the performance of the proposed circuits, We use mentor graphics, tanner tool .The evaluation results of 45-nm CMOS technology shows that the designed circuits have best speed and power than design of any full adder .The designed Full Adders has 2-28% increment in terms of energy consumption and PDP than of other circuit schematics.

KEYWORDS: FULL ADDER (FA), XOR-XNOR

1. INTRODUCTION

In today's world, now day's electronic systems play a crucial role in everyday life. As the demand for electronic systems increases, the usage of circuits is restricted to consume low power and energy consumption. Therefore, as their is growth in population and technology the demand for the portable devices have increased a lot ,so the designers to meet the above requirement ,designs the circuit which consumes low energy consumption and area with the increase of speed. As the digital systems are designed to perform arithmetic operations, such as adder circuits, multipliers circuits and dividers schematics. As the technology is developed the chip density for the design of circuit is increased. So the plenty of transistors are doped into the single chip.

Full Adder schematics are divided into full-swing and non full-swing types. The output of the full adder is driven by the Standard CMOS, complementary pass-transistor logic (CPL) , transmission gate (TG) , transmission function, and hybrid pass logic with static CMOS. In full swing family the FA are most important. Non full-swing type consists of 10T and 8T . In this project, we simulate for the XOR or XNOR and both XOR and XNOR gates and provides new schematics for both . Also, we resolve the issues that are present in the investigated schematics. Later, we proposed the six new full adder architectures with new XOR/XNOR and XOR-XNOR.

In this project we are designing a low power CMOS full adder. As in recent times we identified that the low power design of VLSI circuits play a crucial role in critical technology, which has a huge demand of portable consumer electronics products in recent years. So in this process many enhanced circuits came into picture for designing basic logic functions using pass transistor and transmission gates. The proposed new schematic can operate within the applied condition whenever the power supply voltage is reduced, and this is considered to be continued until it is given to the initial design step of sizing the MOS transistors. so to overcome this , by the new XOR-XNOR gates.

2. LITERATURE SURVEY

In this project a low power 1-bit CMOS full adder is designed .Here the full adder circuit are

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categorized into different modules and modules are verified and observed. The smaller modules are designed and developed, prototyped, simulated and analyzed. Here we are designing different full adder's circuits by using these modules. Each of the designed 1-bit full adder circuit exhibit different energy consumption, speed, area and driving capability. As the design of low power VLSI systems demand in fast growth technologies in mobile communication .But there is a limitation for consuming the power for the systems. so designers are facing problems of low energy consumption. So to overcome this high performance low power full adder schematics are designed. In most of the system the full adder is main block that shows the overall execution of the circuits. That is reason here we are choosing the evaluation of the 1-bit full adder circuit.

In this project a CMOS full adder by using the transmission theory is proposed .Here we are implementing two CMOS full adder are designed. The designed two full adder are similar in circuit design than the standard full adder. As the full adder is the main block for arithmetic operation it provides a best specifications to modify the system of full adder. The serial connection for full adders is limited as the full adders do not have the driving outputs. The CMOS transmission gate cannot be presented with AND, OR, and NOT operation in boolean algebra as output is inverts the input. In boolean algebra the high input impedance is not defined. using switching level of a MOS transistor the CMOS full adders are designed .To overcome this here we are using transmission function theory ,to explain the logic function of the full adder and CMOS full adder schematics can be modified.

In this project a low complexity full adder higher performance analysis low power energy consumption is designed. In this process we design XOR and AND gate pass transistor and transmission gates by using low power design technique..In conventional we use 16T where as in proposed model we use 10T.To overcome the sub threshold current leakage we are designing proposed model. The proposed circuit has reduced threshold problems, high speed, low energy consumption and noise gain over the 10T full adder .when compared with standard and improved full adder the energy consumption is decreased to a larger part and area is reduced. Energy saving may be upto40% may be achieved. We also explained how XOR and AND gates are used to drive the full adder schematic .The evaluation characteristics of the full adder is verified and simulation results are obtained from tanner tool.

3. DESIGN AND SIMULATION

The two input signal A,B are given to transistors.the signal B is given to P2 and signal A is given to P3.The signal B is given to N2 and P4 and the signal a is given to N2 and N3.The N3 is connected to P4.The signal B is given to N4 and P6 and the signal A is given to P5 and P6.

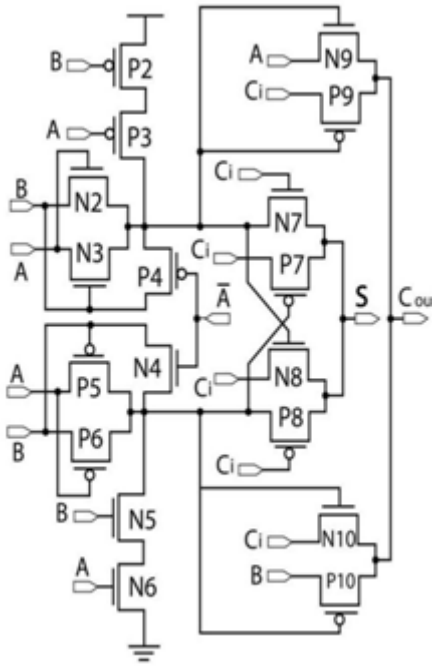


Figure 1: Hybrid Full Adder-20 Transistor

The N4 is connected to N5.The signal B is given to N5 and the signal A is given to N6.The transistors P4 and N4 are shorted together and the out is A_{bar}.The signal A is given to N9 and C_i is given to P9.The N2 and N3 transistors are shorted together and output is given N7 and C_i is given to N7, C_i is given to P7.the N2 and N3 transistors are shorted together and output is given N7 and N8. The P5 and P6 transistors are shorted together and output is given P7 and P8 C_i is given to N8,P8.the output to N2 and N3 is given to N9 and P9 and output of P5 and P6 is given to N10 and P10.The signal C_i and B is given to N10 and P10.The output of N7 and P7 and output of N8 and P8 are shorted together and the output is sum. The output of N9,P9 and N10,P10 are sorted together and output is carry.

The input signal A is given to inverter which consists of P1 and N1 transistors. Carry signal C_i is given to inverter which consists of P2 and N2 transistor. The signal A is given to P3,P2 and signal B is given P2,N4.The output of P3,P2 are shorted together and is given to N4,the N4 is connected to N3.The signal A is given to N3 and signal B is given to N2.The output of P3,P2 is given to inverter which consists of P4 and N5.The output of inverter is given to N6,N7,N8,P7.

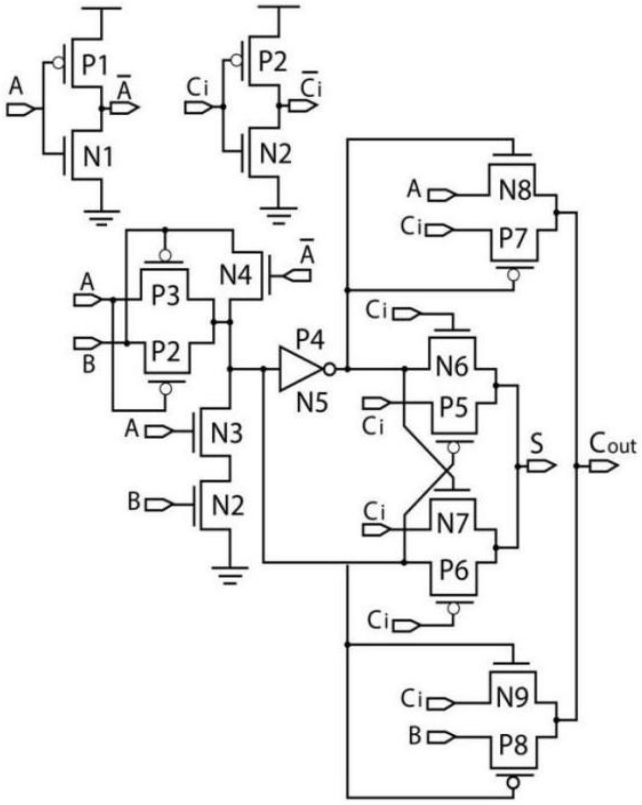


Figure 2: Hybrid Full Adder 17 Transistor

The signal C_i is given to N6,P5,N7,P6,N9,P7.The input of inverter is given P6 ,P5,N9 and P8.The output of transistors N6,P5 and N7,P6 are shorted together .The output is sum.The output of N8,N7 and N9,P8are shorted together and the output is carry.

The signal A,B are given to P4,P3.The transistor P4 is connected P5.The signal B is given to N3 and P5.The signal A is given to N3 and N4.The signal A is given to P6 and P7 .The signal B is given P7 and N5.The transistor N5 is connected N6.The signal B is connected N6 and the signal A is connected to N7.The output of P5 and N5 is $A_{bar.}$The output of N3 and N4 is given N8 , P9,N10 and P11.The output of P6 and P7 is given to P10,N11,P8 and N9.The signal A_{bar} is given to p8 and n8.

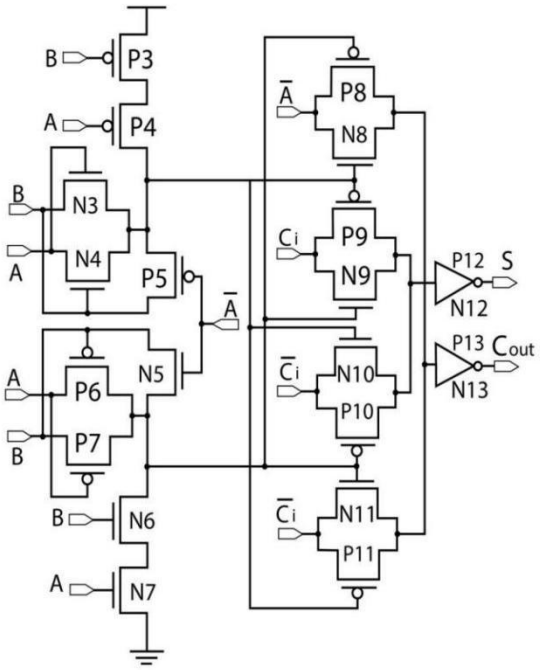


Figure 3: Hybrid Full Adder 26 Transistor

The signal C_i is given P9 and N9.The signal C_{ibar} is given N10 and P10.The signal C_{ibar} is given N11 and P11.The output of N9,P9 and N10,P10 are shorted together and is given to inverter which consist of P12 and N12 ,the output of inverter is sum. The output of N8,P8 and N11,P11 are shorted together and is given to inverter which consist of N13 and P13 ,the output inverter is carry**.**

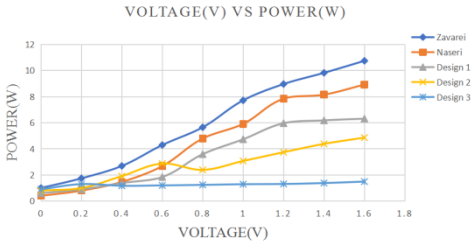
4. RESULT

The standard full adders proposed here are examined and evaluated and reveals that there are some drawbacks ,considering this as a task and challenge we rectify the issues The simulation results of existing and proposed methodology was shown in table 1 which is the comparison factor of power, PDP, delay. In existing design and other old papers they used 65nm technology. In this paper we are using 45nm technology for simulation of standard and proposed full adder ,we are getting the effective results for power, delay, PDP. With the effective values considering from the table we are plotting graphs for voltage Vs power; voltage Vs delay and along with voltage Vs PDP.

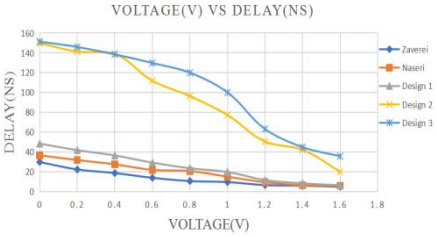
TABLE-1: Comparison Of Power ,Delay, Pdp With Existing And Proposed Technology

	Existing Technology with 65nm			Proposed Technology with 45nm		
	Power (W)	Delay (ns)	PDP	Power (W)	Delay (ns)	PDP
Design-1	10.46	55.8436	340.9870	6.31	48.43n	305.8782
Design-2	7.98	190.8456	805.7815	4.86	149.7216	728.7686
Design-3	3.69	210.5680	291.1505	1.4	151.4230	223.3075

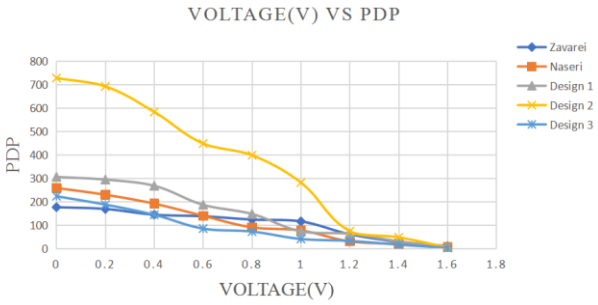
Here the proposed technology with 45nm is better than the existing technology with 65nm of design-1 in terms of power which is reduced from 10.46w to 6.31w ,delay reduced from 55.8436n to 48.43n and PDP from 340.9870 to 305.8782. Design-2 in terms of power which is reduced from 7.98w to 4.86w ,delay reduced from 190.8456 to 149.7216 and PDP from 805.7815 to 728.7686.Design-3 in terms of power which is reduced from 3.69w to 1.4w ,delay reduced from 210.5680n to 151.4230n and PDP from 291.1505 to 223.3075.



(a)



(b)



(c)

Figure 4: Proposed Graph Simulation Results a) Voltage Vs Power b) Voltage Vs Delay c) Voltage Vs Pdp

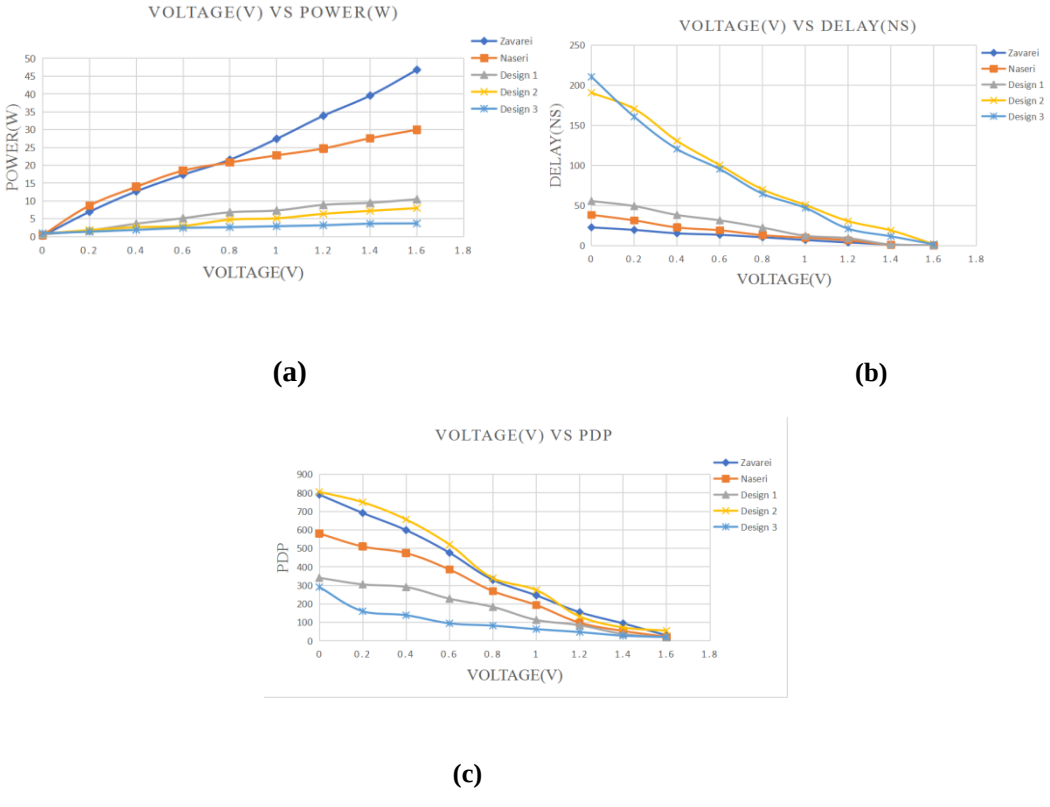


Figure 5: Existing Graph Simulation Results a) Voltage Vs Power b) Voltage Vs Delay c) Voltage Vs Pdp.

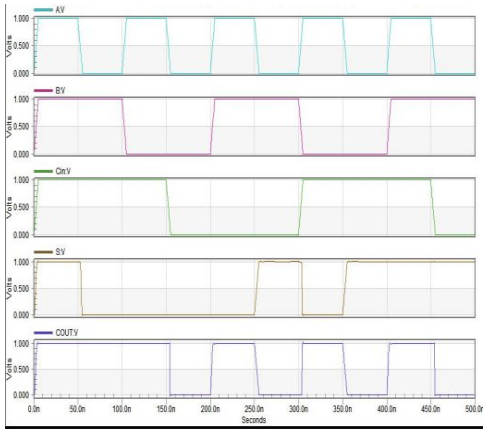


Figure 6: Result of Hybrid Full Adder 20 Transistor

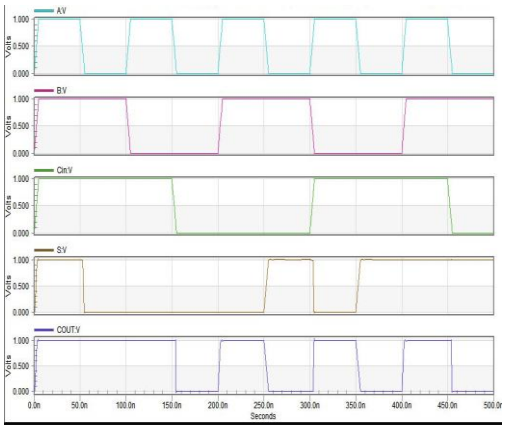


Figure 7: Result of Hybrid Full Adder 17 Transistor

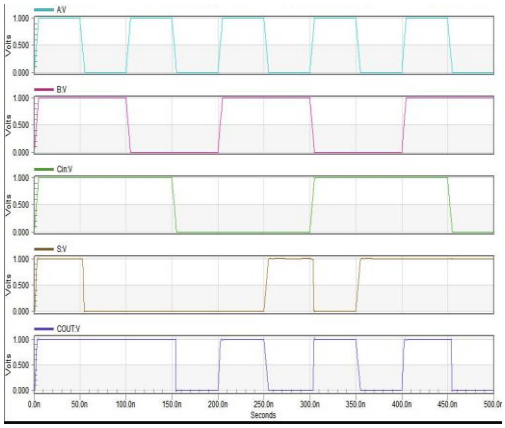


Figure 8: Result of Hybrid Full Adder 26 Transistor

5. CONCLUSION

In this project first we evaluated XOR-XNOR schematics .The simulation shows that the NOT gates in schematic is disadvantage and another disadvantage is positive feedback. Due to this presence of feedback the delay, output capacitance and power consumption are increased .Then we propose new XOR-XNOR schematics that may reduce the above listed drawbacks. We designed three new Full Adder circuits for various algorithms by using new XOR-XNOR gates. The performance of FA schematic in various stages, the results show that the designed schematics has a excellent execution .The designed full adder schematics execution results shows that the PDP is saved up to 23% comparison with other Full Adder circuits. The proposed FA designs have best speed and power.

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